REMARKS

After entry of this amendment, claims 61-80 remain pending. In the present Office Action, claims 31-42 and 51-60 were rejected under 35 U.S.C. § 102(b) as being anticipated by Turley, Advanced 80386 Programming Techniques ("Turley"). Claims 43-50 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Turley in view of Gulick et al., U.S. Patent No. 5,732,224 ("Gulick"). Claims 52-53 and 57-58 were rejected under 35 U.S.C. § 112, second paragraph. Applicants respectfully traverse these rejections and request reconsideration. In view of cancellation of claims 31-60, Applicants respectfully submit that the rejections are moot.

New Claims

Applicants respectfully submit that each of new claims 61-80 recite combinations of features not taught or suggested in the cited art. For example, claim 61 recites a combination of features including: "the execution core is configured to: (i) use a value of a register address field of the instruction to select a least significant portion of one of the plurality of registers responsive to detecting a prefix field in the instruction... and (ii) use the value of the register address field to select one of *either* a least significant portion *or* a second least significant portion of one of a subset of the plurality of registers responsive to detecting a lack of a prefix field in the instruction, wherein the subset excludes at least one of the plurality of registers". Neither Turley, nor Turley in view of Gulick, teach or suggest the above highlighted features.

Turley teaches a processor that operates in a 32 bit mode (D=1). In the 32 bit mode, for an instruction that includes an operand size override prefix, the processor selects the least significant 16 bits of the specified register (Turley, page 263, first paragraph). For an instruction that does not include the operand size override prefix in the 32 bit mode, the processor selects the entire 32 bits of the specified register (Turley, page 261, last paragraph). The processor also can operate in a 16 bit mode (D=0). In the 16 bit mode, for an instruction that does not include the operand size override prefix, the processor selects the least significant 16 bits of the specified register (Turley, page 262, first paragraph). For an instruction that does not include the operand size override prefix

in the 16 bit mode, the processor selects the entire 32 bits of the specified register (Turley, page 263, second paragraph). None of this teaches or suggests the above highlighted features.

Applicants submit that claim 61 is patentable over the cited art. Claims 62-64 depend from claim 61 and recite additional combinations of features not taught or suggested in the cited art. Each of claims 65, 69, and 73 recite combinations of features including features similar to those highlighted above with respect to claim 61. Accordingly, Applicants submit that each of claims 65, 69, and 73 are patentable over the cited art. Claims 66-68 depend from claim 65 and recite additional combinations of features not taught or suggested in the cited art. Claims 70-72 depend from claim 69 and recite additional combinations of features not taught or suggested in the cited art. Claims 74-80 depend from claim 73 and recite additional combinations of features not taught or suggested in the cited art.

The present Office Action states that "because the operand-size override prefix byte does not affect instructions that include one byte operands, and instruction can specify a one byte operand and the operand-size override prefix byte causing a mapping to a least significant (lower 8 bits) of any of the registers to be created" (Office Action, page 6, lines 1-4). **Applicants respectfully submit that Turley does not contain the above highlighted teachings**. Absent an explicit teaching of a mapping to a least significant (lower 8 bits) of any of the registers, Applicants respectfully submit that the above assertion from the Office Action is unfounded and not supported in Turley.

Drawing Objection

The present Office Action objected to the drawings for not showing a modem, a network interface device, and an audio device. Applicants respectfully submit that the drawings, as filed, meet the requirements of 37 C.F.R. § 1.83(a). Nevertheless, Applicants have amended Figs. 13 and 14 to list the above devices as examples of the PCI device 212A, the ISA device 218, and the I/O device 320B in accordance with the description of these devices in the specification. See, e.g., specification, page 33, line 28-

page 34, line 6 and page 37, lines 22-29. In addition, Applicants have amended Fig. 2 to insert the label "EDI" next to the last register. Applicants submit that this amendment is supported in the application as filed, in the description of the registers as defined in the x86 instruction set and further as shown in Fig. 4. Applicants believe that no new matter has been entered.

CONCLUSION

Applicants submit that the application is in condition for allowance, and an early notice to that effect is requested. If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-66100/LJM.

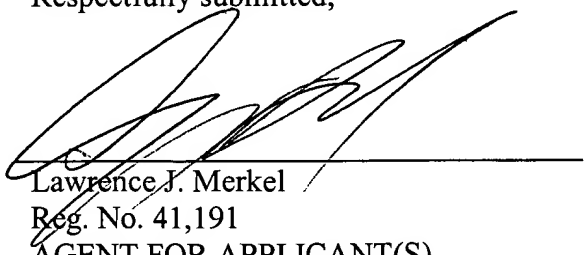
Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Fee Authorization Form authorizing a deposit account debit in the amount of $ for fees ( ).

☒ Other: 3 Replacement drawing sheets (Figs. 2, 13, and 14)

Respectfully submitted,



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Date: 9/2/04

IN THE DRAWINGS:

Attached hereto are 3 replacement drawing sheets, replacing Figs. 2, 13, and 14 as currently on file. Changes to the drawings are described below.